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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/006,860	12/04/2001	Yuichiro Miyamoto	MTS-3296US	8913

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EXAMINER	
THOMAS, SHANE M	

ART UNIT	PAPER NUMBER
2186	9

DATE MAILED: 04/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/006,860	MIYAMOTO ET AL.	
	Examiner	Art Unit	
	Shane M Thomas	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-6 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) 1 is/are allowed.

6)☒ Claim(s) 2-6 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 28 January 2004 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

The Examiner's objections to the drawings have been withdrawn hereto.

Specification

The Examiner's objections to the specification have been withdrawn hereto.

Claim Objections

The Examiner's objections to the claims have been withdrawn hereto.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Graef et al. (U.S. Patent No. 6,101,329) in view of Yu (U.S. Patent Application Publication No. U.S. 2001/0043603) in further view of Brauch et al. (U.S. Patent No. 6,550,023).

(From Non-final action) Graef shows an asynchronous FIFO circuit in figure 1 comprising a memory 12 and data write element 10 and data read element 11. The read and

write elements operate at different data rates, hence asynchronous operation (column 3, lines 15-18). Graef's asynchronous FIFO circuit continuously monitors multiple counter blocks, tracking pointer positions to the storage locations of the fifo memory, and flag registers that indicate full and empty conditions of the FIFO circuit. However, Graef does not monitor nor compare the reading or writing of data containing errors. Yu discloses in his FIFO system a teaching of using a performance monitoring method to record and count errors in the receive FIFO (RXFIFO) and the transmit FIFO (TXFIFO). Outgoing data (*read* data from the FIFO) from the RXFIFO is marked as "errored" and accumulated by the performance monitors (¶ 149). Additionally, performance monitoring is performed for packets discarded due to RXFIFO errors (¶ 153). In the TXFIFO, packets are received (data is *written* into the FIFO) (¶ 196), and performance monitors count the number of FIFO error events (¶ 183). Specifically, an 8-bit FIFO error counter counts every packet affected by a FIFO error event (¶ 199). Since the --Performance Monitor-- of Yu uses an error counter to count the number of errors in the TXFIFO, the examiner is interpreting that the --Performance Monitor-- uses a counter means for the RXFIFO as well since the errors are *accumulated* by the --Performance Monitor--. Thus is can be seen that the --perfomance monitors-- count errors when data is read (RXFIFO) and written (TXFIFO). Further, using the example of Yu in ¶ 200, since the FIFO error counter counts every erroneous packet, the examiner is considering that the 8-bit counter increment by 1 bit after every invalid packet.

(Non-final action) Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the asynchronous FIFO circuit of Graef with the teaching of Yu in order to have gained the benefit of monitoring the reading and writing

performance of the FIFO circuit for errors by means of counting the errors. The FIFO circuit upon detecting corrupt, invalid data could have therefore performed operations to the invalid data such as aborting the corrupt data as Yu mentions in ¶ 200. Such an operation would have increased the reliability of the asynchronous fifo circuit of Graef by having been able to discard or mark invalid data.

(Non-final action) The teaching of Yu does not disclose a comparison means for comparing the counters containing the number of errors from the data written into and read from the FIFO memory 12 of Graef. Braud teaches a bit comparison technique in column 2, lines 40-52, such that if the corresponding bits of two data registers coincide, a logic 0 is produced; likewise, if the contents of the registers do not coincide, then a logic 1 is produced from the comparing means. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify the asynchronous FIFO system of Graef with the teaching of Braud so that the determination could have been made as to when data packets (that were affected by an error event when written into the FIFO memory) have been read out (both write and read error counters being equal). Such a feature would have been useful when determining if invalid data remained in the FIFO memory after being written in; having counters that do not coincide would have indicated that invalid data remained in the FIFO memory.

(NEW) Regarding the amended portion of claim 4:

wherein the logic level of 1 indicates at least one error flag is set in the predetermined amount of data stored in the memory

Yu further states in ¶149 that outgoing data is *marked as errored* if an FCS error is detected. The Examiner is considering marking the data to be equivalent to setting an error flag since in order to have *marked* data an indication must have been set in order to distinguish the associated errored data from valid data. Therefore, in accordance with the discussion above, it would have been seen by one of ordinary skill in the art that the logic level of 1 would have indicated at least one error flag (or error indication via a *mark* as taught by Yu) is set (*marked*) in the data that is stored in the memory (FIFO of modified Graef).

Claims 2,3,5, and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Graef et al. (U.S. Patent No. 6,101,329) in view of Yu (U.S. Patent Application Publication No. U.S. 2001/0043603), as applied to claim 4 above, in further view of Brauch et al. (U.S. Patent No. 6,550,023) in further view of Bastiani et al. (U.S. Patent No. 6,609,169) in further view of the applicant's admitted prior art.

(Non-final action) As per **claims 2 and 5**, Graef shows write counters 18-20 and read counters 21-23 in figure 1. Graef discloses the operation of the counters in column 6, lines 9-52. The write counters (denoted by Graef as W, W+1, and W+2) are incremented by 1 if the FIFO memory is not in a full state and a write operation is issued. Likewise, the read pointers (denoted as R, R+1, and R+2) are incremented by 1 if the FIFO memory is not in an empty state and a read operation is issued.

(Non-final action) Further Graef discloses an empty flag 16 and states in column 4, line 35-39, that when the read and write pointers are coincident, the empty flag is set.

(Non-final action) Greaf discloses a full flag 15 and monitors the maximum capacity (denoted by Graef as B) of the FIFO to determine when to set the full flag (column 4, lines 8-27). Applicant's invention uses the value of a --previous read pointer-- and comparing it to the value of write pointer in order to determine the status of the full flag. Graef does not disclose a --previous read pointer--; however, the operation of the FIFO circuit of Graef and the FIFO circuit of the applicant exhibit equal performance. Both determine when the FIFO memory is full and set the full flag. Additionally, the --previous read flag-- is used by the applicant to read out previously read out data if a read operation is issued and the FIFO memory is empty (empty flag is set) so that invalid data is not read out (¶ 116 of Applicant's disclosure). The operation of the prior art (Graef) blocks read operations if the empty flag is set, thus not allowing invalid data to be read out (column 4, lines 39-41). Therefore it could have been seen by one having ordinary skill in the art that both the prior art and applicant's invention are performance equivalents when determining full flag status and when blocking the reading of invalid data.

(Non-final action) A --write pointer decoder-- for decoding the write counter when a write operation is issued and a --data selector-- for selecting data from an address specified by the read pointer when a read operation is issued are both inherent components of a FIFO circuit. Since the write pointer points to the location in the FIFO memory where the next packet of data will be stored, there must be some form of decode logic used to determine which location in the FIFO memory to which the write pointer is pointing to. Likewise, the read pointer must be decoded in a similar fashion and data selected from one of the FIFO memory locations corresponding to the address contained in the read pointer.

(Non-final action) Graef does not disclose OR circuits used to take a --logic sum-- of bits in the data written to or read from the FIFO memory. The applicant's admitted prior art shows in figure 9, that each entry into the FIFO memory contains data bits and error bits. Further, in figure 10, applicant shows the admitted prior art logically ORing the two error bits, thus obtaining a --logical sum-- of the two error bits. This process would have allowed the asynchronous FIFO circuit of Graef to determine if a given data entry had an error associated with it (either of the error flags had been set). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify the asynchronous FIFO circuit of Graef, using the teaching of the applicant's admitted prior art, in order to determine if a given entry in the FIFO memory contained data associated with an error at the times when the data was written into and read out of the FIFO memory.

(Non-final action) Regarding lines 2 and 5 of claims 2 and 5, respectively, Graef does not impose a specific size constraint of the asynchronous FIFO 12 in figure 1. Bastiani states in column 56, lines 19-26, that FIFO buffer size can be chosen based on an array of design criteria such as packet size and link transfer rate. As can be seen on the right side of Table 58 of column 55, the FIFO sizes are all base-2 logarithms. The examiner is considering 1 byte words; therefore N would equal, 6,7,8,9,10, and 11 for the respective table entries. In other words, for a 64-byte FIFO (first entry of Table 58) the number of addresses in the FIFO would be 2^6, and for a 128-byte FIFO, the number of addresses would be 2^7. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the asynchronous FIFO of Graef with the teaching of FIFO size of Bastiani in order to design the FIFO size so that overruns and underruns would have been less likely to have occured (column

55, line 26 of Bastiani). Further in the applicant's admitted prior art, the applicant makes references on page 1 to dual 16-word FIFO asynchronous circuit, PC16550D, which uses 16-word (2^4) address locations, with N=4. Dual FIFO OX16C950, discussed on page 3 use 128-word (2^7) address locations, with N=7 in this case.

(Non-final action) The rejection for claim 2, lines 32-41, and claim 5, lines 33-42, follows claims 3's rejection above.

(NEW) Regarding the amended portion of claims 2 and 5, lines:

wherein the error comparing circuit outputs a logic level of 0 when the value of said error write counter is coincident with the value of said error read counter and said error comparing circuit outputs a logic level of 1 if the former value is different from the latter value

(NEW) The rejection for this limitation follows the rejection for claim 4, lines 10-14, above, found in the teaching of Brauch in column 2, lines 36-46. Brauch teaches a method of outputting a 0 if the inputs are the same and a 1 if they are different.

(NEW) Regarding the amended portion of claims 2 and 5, lines:

the logic level of 1 indicates at least one error flag is set in the data [predetermined bits] stored in the memory

Yu further states in ¶149 that outgoing data is *marked as errored* if an FCS error is detected. The Examiner is considering *marking the data* to be equivalent to setting an error flag since in order to have *marked* data an indication must have been set in order to distinguish the associated errored data from valid data. Therefore, in accordance with the discussion above, it would have been seen by one of ordinary skill in the art that the logic level of 1 would have

indicated at least one error flag (or error indication via a *mark* as taught by Yu) is set (*marked*) in the data that would have been stored in the memory (FIFO of modified Graef).

(Non-final action) As per **claims 3 and 6**, Graef teaches and uses gray counters in his asynchronous FIFO circuit. He teaches in column 5, lines 26-39, that using gray counters in an asynchronous circuit, provide a shorter settling time since they toggle less pins in the circuitry and can ultimately settle with fewer data spikes, helping to prevent spurious read and write enable requests. Therefore it would have been obvious to one having ordinary skill in the art at the time in the invention was made to use gray counters for the error read and error write counters of the modified asynchronous FIFO circuit of Graef in order to reduce the number of data spikes when the error counters are incremented, thereby increasing the reliability of the error counters.

Allowable Subject Matter

Claim 1 is allowable over the prior art of record. The following is a statement of reasons for the indication of allowable subject matter:

The combination of Graef, Yu, Brauch, Bastiani, and the Applicant's admitted prior art, fail to teach *each* word of a plurality of words [stored in a respective plurality of address locations in an asynchronous fifo memory] wherein each word of the plurality of words contains an error flag. The teaching of Yu, teaches away from associating an error flag with *each* word in that ¶183, ¶199, and figure 4 imply that errors are associated with whole frames (figure 4), which the Examiner has considered to be --predetermined amount of data-- in the rejections above.

Further, the --performance counters-- of Yu, which the Examiner as considering as error counters, count the errors for the packets that would have been transmitted (¶199).

Response to Amendment

In response to the Applicant's amendment, filed 28 January 2004, the Examiner has stated allowable subject matter for claim 1 and has withheld the rejections of claims 2-6.

Regarding amended claims 2-6, the Examiner has cited teachings of Yu that teach the Applicant's amended limitations.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shane M Thomas whose telephone number is (703) 605-0725. The examiner can normally be reached on M-F 8:30 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt M Kim can be reached on (703) 305-3821. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shane M. Thomas

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